Abstract of the Disclosure

A sense amplifying circuit and a bit comparator having the sense amplifying circuit. The sense amplifying circuit may include a selecting unit, a sensing unit, a latching unit, an output unit, and a switching unit. The selecting unit may select one pair from a first pair of a first signal and a first inverted signal and a second pair of a second signal and a second inverted signal, in response to a selection signal and an inverted selection signal. The sensing unit may sense voltage levels of one pair of signals selected from the first pair and the second pair. The latching unit may precharge first and second nodes in response to a clock signal and controls voltage levels of the first and second nodes in response to a sensing result of the sensing unit. The output unit may invert the voltage levels of the first and second nodes to generate first and second output signals. The switching unit is capable of controlling the operation of the selecting unit in response to the clock signal.